DEVELOPMENT OF IPA-FREE TEXTURING PROCESSES IN ADVANCED SOLAR CELL FABRICATION

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ABSTRACT: The application of IPA-free alkaline solutions to replace an existing IPA-usage texturization process for the fabrication of advanced silicon solar cells in a large-scale production line is developed and evaluated. A non-IPA additive with KOH solutions was employed and process parameters were modified for texturing 156mm n-type c-Si wafers to produce texture morphologies similar to those with KOH/IPA solutions. The wafers were then made into advanced cells in a heterojunction (HET) solar cell fabrication pilot line. Conversion efficiency of the cells from the IPA-free KOH texturized wafers was compared to the KOH/IPA texturized wafers. Wafers processed in an IPA-free KOH bath with different extents of bath life and in baths with various silicate levels were also evaluated. No noticeable changes in cell performance were observed. Overall, the experiments showed that an IPA-free KOH texturing process can be optimized to integrate with an existing HET cell production line without the need of re-tuning the parameters of subsequent processes nor compromising the cell performance.

Keywords: silicon solar cells, high efficiency, heterojunction, alkaline texturization, IPA-free additive

1 INTRODUCTION

Heterojunction (HET) solar cells produce relatively high open circuit potential based on the excellent surface passivation of c-Si by intrinsic hydrogenated amorphous Si (a-Si:H). Recently these cells are getting more attraction as a technology to meet the industry's goal of developing high efficiency, low cost solar cells [1-3]. Among the process challenges of manufacturing HET cells, wafer surface preparation with wet chemical processes is recognized to be critical to ensure optimal texture morphology and Si surface quality for the subsequent passivation step to achieve good cell performance [4-5].

Anisotropic etching of Si with alkaline solutions along with IPA has long been used in the industry to texturize (100) oriented monocrystalline silicon wafers for solar cell manufacturing [6-7]. With selective etching of silicon crystal planes by the alkaline etchant, random pyramidal hillocks with (111) facets are formed on the (100) c-Si wafer to reduce the overall surface reflectance for better photon energy absorption in the solar cell [8]. IPA as an additive in the texturing solutions is not involved in the etching reaction but serves as a wetting agent for texturing homogeneity by preventing the H_2 bubbles (i.e. an etching byproduct) from adhering to the Si surface.

In recent years, there have been continuing efforts to develop alternative substances to replace IPA in the alkaline texturing solutions for enhancing the process robustness, reducing the hazard potential, and lowering the operation cost [9-11]. IPA-free additives are already commercially available and used in the industry for Si solar cell manufacturing. However, the additives were mostly developed to produce relatively small and homogeneous pyramids (< 4 µm) in favor of low surface reflectance and quick texturization turnaround (i.e. less Si material loss and higher throughput). For HET solar cells, small pyramids is no longer invariably preferable. Increased densities of peaks/valleys of small pyramids increase the chance of epitaxial growth of the a-Si:H layer and cause a detrimental effect to the effective carrier lifetime and thus cell performance [12-14]. Optimization of the HET fabrication processes such as PECVD and TCO is therefore required [14], or modificaiton of the IPA-free texturing process is needed.

This study was conducted to evaluate the feasibility of introducing an IPA-free alkaline texturing process into an HET solar cell fabrication pilot line currently using KOH/IPA for silicon texturization with little or no disturbance to the existing processes, equipments and cell performance.

2 EXPERIMENTAL

As-cut n-type 156 x 156 mm^2 pseudo-square (PSQ) monocrystalline solar wafers grown with Czochralski (CZ) techniques were obtained from different suppliers and processed in Akrion Systems' Applications Lab. Wet chemical processes for wafer surface preparation were conducted on a fully automated GAMA^{TM} wafer etching and cleaning station. KOH solutions mixed with an IPA-free additive, or IPA, were used for the texturization process. Textured wafers were then sent to a heterojunction solar cell pilot line called "LabFab HET" located in CEA-INES at France [15] to complete the solar cell manufacturing.

The solar fab is equipped with an Akrion Systems' high volume mass production wet station, GAMA-Solar^{TM}. It uses KOH/IPA processes to texturize wafers and applies advanced smoothing and cleaning processes followed by an HF-last treatment to the textured wafers before the PECVD step. Solar wafers from the same suppliers with similar grades were concurrently processed with the GAMA-Solar^{TM} production tool and made to HET cells to serve as process control. Experimental details are given in the following section with respect to specific testing conditions.

3 RESULTS AND DISCUSSION

The approach of the study was to develop an IPA-free texturing recipe in Akrion System's Apps Lab, then to run a small scale of wafers to evaluate the robustness of the process (e.g. bath life, silicate buildup, wafer load, etc.), and then to run multiple batches of wafers using the developed recipe as a best known method (BKM) for statistical analysis.

3.1 IPA-free texturing recipe development

Taking the advantage of high boiling point of the IPA-free additive, a design of experiment (DOE) on process temperature and time was conducted to optimize the texturing conditions for etch depth and reflectance. The aim was also to produce pyramid sizes close to those produced by the current KOH/IPA process of record for HET cells. Figure 1 shows the etch depth and reflectance results of a 4×4 DOE with respect to texturing temperature, T, and process time, t. The optimal condition is associated with the "green" color zone in both maps (e.g. t2 paired with T3), which produces a desired result of pyramid sizes around 10 µm with etch depth of 7.5 – 10 µm and low 9% reflectance at 950 nm wavelength.

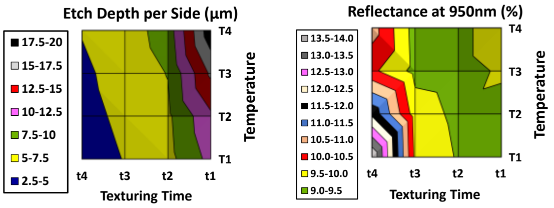

Figure 1: IPA-free texturing processes with DOE splits on temperature and time, showing the etch depth and reflectance for an optimal combination of the parameters

A number of wafers was split to run a standard KOH/IPA, a standard IPA-free KOH, and an optimized IPA-free KOH texturing process, respectively. Figure 2 shows the SEM images of the pyramidal morphologies of each texturing condition and the corresponding quasi steady state photo conductance (QQSPC) passivation results. It is clear that the standard KOH/IPA-free produced small and uniform pyramids but inferior QQSPC results against the standard KOH/IPA condition. The optimized KOH/IPA-free recipe, however, enlarged the pyramid sizes closer to those formed by the standard KOH/IPA process and produced better passivation performance.

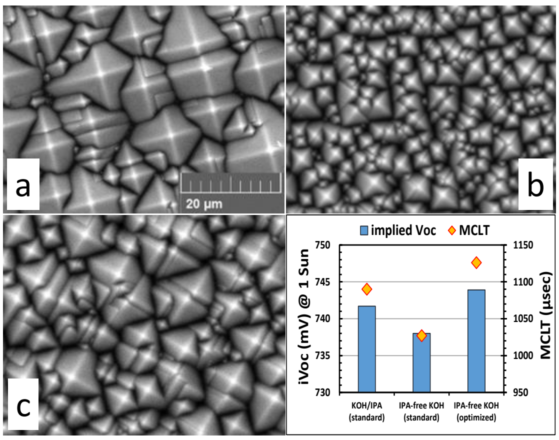

Figure 2: SEM images of texturized wafers with a (a) standard KOH/IPA, (b) standard KOH/IPA-free, and (c) optimized KOH/IPA-free condition and the corresponding QQSPC passivation results in implied Voc and MCLT

As shown in Fig. 3, the conversion efficiency of the HET solar cells made from the three split-groups also showed a similar trend of the benefit of IPA-free KOH texturing process optimization.

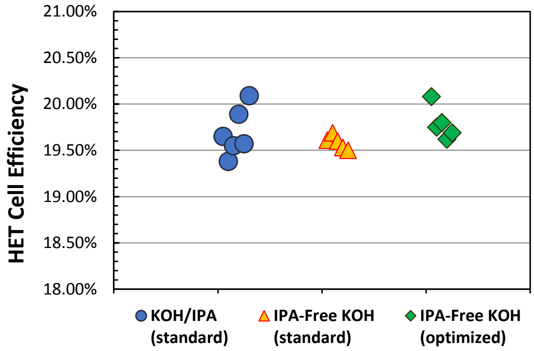

Figure 3: HET cell efficiency of wafers (same wafer grade and supplier) texturized with different conditions, showing the benefit of IPA-free process optimization

3.2 Effects of bath life, silicate level and wafer load

To minimize the mutual influence between the bath life, silicate level, and wafer load to texturization results and cell performance, three distinct texturing baths were prepared in the GAMA^{TM} station of Akrion Systems' lab. Three types of wafers (A, B and C) were used, where A and C are two different grades of wafers from the same supplier, while B was obtained from a different supplier. For bath life evaluation, one batch of wafers mixed with A, B, and C in a partial load was processed when an IPA-free KOH bath was freshly prepared. The bath was then kept in idle without running product except for necessary replenishment to maintain bath's liquid level until its 100-hour life to run the second batch of wafers. The same practice was applied until the 186-hour life to run the third batch. As such, the silicate level in the bath was always kept at a relatively low level (i.e. < 5 g/L). For the silicate level testing, a fresh IPA-free KOH bath was mixed and doped with desired amounts of silicon to generate ~10 g/L and ~20 g/L silicate levels. One batch of partially loaded product was processed in each of the silicate concentrations. For the full wafer load testing, a fresh IPA-free KOH bath was prepared and a batch of full-load wafers mixed with A, B, and C was processed. Figure 4 shows the HET cell performance of the textured wafers (B type) along with a batch of B type LabFab control.

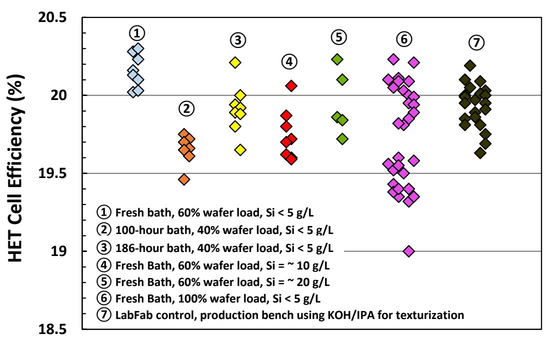

Figure 4: HET cell efficiency of type-B wafers texturized with the optimized IPA-free recipe in a fresh bath (group ①), 100-hour bath (group ②), 186-hour bath (group ③), 10 g/L silicate level (group ④), 20 g/L silicate level (group ⑤) and full wafer load (group ⑥) versus the LabFab control (group ⑦)

The data indicates that the optimized IPA-free texturing recipe overall produced results in line with those by conventional KOH/IPA processes. The cell efficiencies at the 100-hour bath life were lower than those when the bath was fresh, but this seemed not to be a trend since the efficiencies at the 186-hour bath life got higher again. The full wafer-load batch also showed good cell performance but with a somewhat larger dispersion. Given that the wafers were texturized in Akrion Systems and transported to CEA-INES for subsequent processes, further investigation will be needed to clarify if these observations are intrinsically IPA-free texturing-related or due to other exterior factors.

3.3 Marathon runs with IPA-free texturing BKM

Multiple batches of wafers of type-A, type-B and type-C were texturized with the KOH/IPA-free BKM in Apps Lab and then shipped to LabFab for cleaning and HET cell fabrication. Both Akrion Systems wet processing tools in each place are equipped with an NIR chemical analyzing unit for concentration monitoring and process control.

Figure 5 is a recording chart of the GAMA^{TM} station in the Apps Lab on which a 4-day marathon texturing test was applied to 1400 type-A wafers. From the data, it can be seen that both the texturing etch depth and texture surface reflectance remain consistent from lot to lot in spite of the silicate buildup in the bath (i.e. up to 25 g/L). It was intentional to change out the texturing bath at the end of the third testing day to qualify the bath-to-bath performance consistency. As shown in Fig. 5, the silicate buildup level, which indicates the amount of silicon being etched, and wafer etch depth as well as reflectance obtained from the fresh bath in the 4th testing day operation is totally consistent with the results from the fresh bath of the 1st testing day.

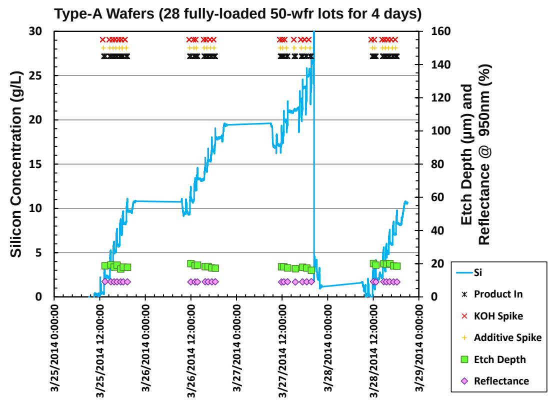

Figure 5: Operational records associated with texturing results of a 4-day marathon test on 1400 type-A wafers, showing consistent etch depth (green squares) and reflectance (purple diamonds) from lot to lot and bath to bath in spite of silicate building up (blue line)

All IPA-free textured wafers from Akrion Systems were then processed in the LabFab along with in-house KOH/IPA control to HET cells. Global data of the solar cells from type-A, type-B and type-C wafers were collected and summarized in Fig. 6. The results indicate that in a production-scale level the optimized IPA-free texturing process is comparable to the conventional KOH/IPA process in terms of cell performance. For example, given the multiple lots of wafers from mixed ingots, the average cell efficiency of IPA-free textured type-A wafers was 20.02% ± 0.37% (1 sigma standard deviation from 374 samples) versus 20.06% ± 0.27% upon 143 KOH/IPA reference samples. For type-B wafers, average cell efficiency of IPA-free textured wafers was 19.93% ± 0.22% upon 108 samples versus the KOH/IPA reference of 19.96% ± 0.15% upon 100 samples. For type-C wafers, it was 19.83% ± 0.19% (34 IPA-free textured samples) versus 19.94% ± 0.33% (225 KOH/IPA reference samples).

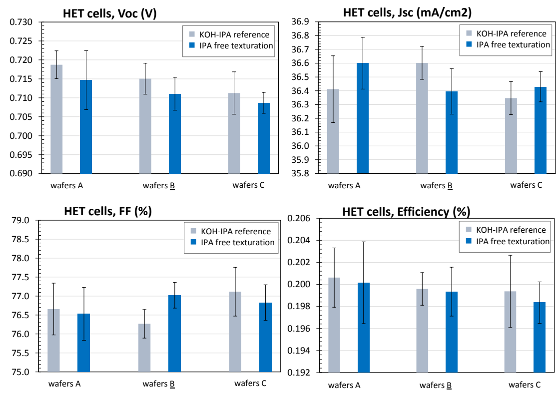

Figure 6: Global HET cell data between IPA-free textured wafers and conventional KOH/IPA textured wafers showing comparable performance

4 CONCLUSION

The application of IPA-free alkaline texturization for the fabrication of heterojunction silicon solar cells in large scale production is developed and evaluated. A non-IPA additive with KOH solution was used and the process parameters were optimized for texturing 156mm n-type c-Si wafers to produce pyramid size similar to those with KOH/IPA solutions. The wafers were then made into HET cells in an industrial pilot line. Conversion efficiency of the cells from the IPA-free KOH texturized wafers was comparable to the KOH/IPA texturized wafers. Overall, the experiments indicated that an optimized IPA-free alkaline texturing is feasible for manufacturing advanced solar cells in an existing KOH/IPA production line. Additional advantages of using non-IPA additive against IPA were also observed, which are significantly improved stability and productivity of the texturization process and increased uniformity of the texture morphologies.

REFERENCE

[1] D-H. Neuhaus, A. Münzer, "Industrial silicon wafer solar cells", *Advances in OptoElectronics*, Vol. 2007, Article ID 24521, 15 pages. http://dx.doi.org/10.1155/2007/24521

[2] S. Gluntz, et al., "N-type silicon enabling efficiencies > 20% in industrial production", *Proc. 35th IEEE PVSC*, Honolulu, HI, USA, 2009, pp. 50 – 56.

[3] S. Harrison, et al., "Towards industrialization of a-Si:H/c-Si heterojunction cells: from 20.5% record cells to 19.8% efficiency on industry compatible

148.5cm^2 CZ wafers", *Proc. 37th IEEE PVSC*, Seattle, WA, USA, 2011, pp. 1444 – 1447.

[4] A. Danel, et al., "Surface passivation of c-Si textured wafer for a-Si:H/c-Si heterojunction solar cells: correlation between lifetime tests and cell performance", *Proc. 26th EU PVSEC*, Hamburg, Germany, 2011, pp. 2260 – 2263.

[5] I. Kashkoush, et al., "Wafer surface preparation for high efficiency solar cells", *Proc. 40th IEEE PVSC*, Denver, CO, USA, 2014, to be published.

[6] D.L. King, M.E. Buck, "Experimental optimization of an anisotropic etching process for random texturization of silicon solar cells", *Proc. 22nd IEEE PVSC*, Las Vegas, NV, USA 1991, pp. 303 – 308.

[7] E. Vazsoni, et al., "Improved anisotropic etching process for industrial texturing of silicon solar cells", *Solar Energy Materials and Solar Cells*, 57, nº 2 (1999), pp. 179 – 188.

[8] J. Hylton, et al., "Alkaline etching for reflectance reduction in multicrystalline silicon solar cells", *J. Electrochem. Soc.*, 151, nº 6 (2004), pp. G408 – G427.

[9] K. Mayer, et al., "New surfactants for combined cleaning and texturing of mono-crystalline silicon wafers after wire-sawing", *Proc. 23rd EU PVSEC*, Valencia, Spain, 2008, pp. 1109 – 1113.

[10] K. Birmann, et al., "Fast alkaline etching of monocrystalline wafers in KOH/CHX", *Proc. 23rd EU PVSEC*, Valencia, Spain, 2008, pp. 1608 – 1611.

[11] E. Wefringhaus, A. Helfricht, "KOH/Surfactant as an alternative to KOH/IPA for texturisation of monocrystalline silicon", *Proc. 24th EU PVSEC*, Hamburg, Germany, 2009, pp. 1860 – 1862.

[12] H. Fujiwara, M. Kundo, "Impact of epitaxial growth at the heterinterface of a-Si:H/c-Si solar cells", *Appl. Phys. Lett.*, 90 (2007), pp. 013503 – 013503-3.

[13] L. Fesquet, et al., "Modification of textured silicon wafer surface morphology for fabrication of heterojunction solar cell with open circuit voltage over 700 mV", *Proc. 34th IEEE PVSC*, Philadelphia, PA, USA, 2009, pp. 754 – 758.

[14] J. Kegel, et al., "IPA-free textured a-Si:H/c-Si heterojunction solar cells exceeding 20% efficiency", *Proc. 28th EU PVSEC*, Paris, France, 2013, pp. 1093 – 1098.

[15] S. Harrison, et al., "CEA-INES heterojunction solar cells 'LabFab' pilot line: production capability demonstrated on 32,000 cells with average efficiency over 20%", *Proc. 29th EU PVSEC*, Amsterdam, The Netherlands, 2014, to be published. .