

The Application of DI-O₃ Water on Wafer Surface Preparation

Gim S. Chen

AKrion, LLC

6330 Hedgewood Dr., #150

Allentown, PA 18106, USA

Abstract – Due to the continuously decreasing scale of integrated circuits (IC) and the increasing requirement in cost-of-ownership (CoO) reduction, throughput improvement and environmental friendliness, endeavor of developing innovative technologies in semiconductor device manufacturing has never ceased. Recent introduction of ozone technology in silicon wet cleaning processes to replace the conventional RCA methods has attracted interest from the industry but apparently deserves more attention for commercial utilization and implementation. In this paper, the application of ozonated DI water (DI-O₃ water) in silicon wafer surface preparation, including removals of organic impurities, metallic contaminants and particles as well as photoresist stripping, is reviewed. The economic advantage of this technology in terms of the savings of chemicals and DI water is also briefly discussed.

INTRODUCTION

The importance of clean substrate surfaces in the fabrication of solid-state microelectronic devices has been recognized since the origin of semiconductor technology. Aggressive chemistries based on the use of strong inorganic acids, bases and oxidizers, such as SPM (H₂SO₄ + H₂O₂), APM (NH₄OH + H₂O₂), HPM (HCl + H₂O₂), HF, etc., have been applied extensively in wet cleaning processes to remove photoresists, particles, light organics, metallic contaminants, and native oxides on silicon wafer surfaces [1]. However, as the scale of silicon circuits and device architectures continuously decreases (from VLSI to ULSI technology, for instance), research and development on exploring effective and reliable cleaning methods to achieve better wafer surface qualities have never been decelerated. On the other hand, in order to meet the increasingly stringent requirements of low cost-of-ownership (CoO) and high environment/safety regulatory standards, the innovation of cleaning technology is also in strong demand.

Ozone has been appreciated due to its strong oxidizing power and is commonly utilized in waste treatment and drinking water sterilization industries. Recent introduction of ozone in semiconductor wet cleaning processes attracts increasing interest, since the technology has proven highly promising for industrial application by meeting many aspects of the aforementioned needs. As shown by the potential-pH diagram in Figure 1, ozonated ultrapure-water (UPW) features higher reduction-oxidation (redox) potential than those of H₂SO₄, HCl, HNO₃ and NH₄OH which have long been used in the conventional wet-cleaning methods [2]. The strongly oxidizing power, in this context, renders ozonated water again a satisfactory agent, by either working alone or mixing with other chemicals, for

the wet cleaning process in semiconductor manufacturing. With proper applications, it can eliminate the use of some highly corrosive chemicals which need to operate at elevated temperatures and, accordingly, reduces the CoO including chemicals expense, rinsing water amount, safety concerns, problems of acid handling and waste processing, etc.

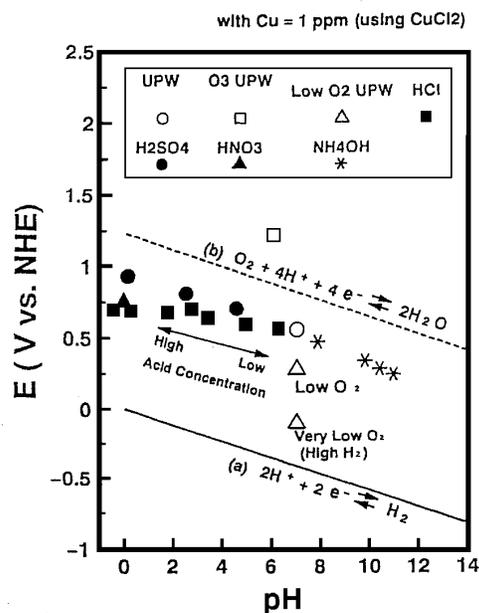


Figure 1. The potential-pH relationship of ozonated water and some chemicals commonly used in semiconductor wet processing. (Ref. 2)

While promising results have been published and commercial tools are also available, the implementation of wet ozone cleaning technology in the semiconductor industry is still limited nowadays. The purpose of this paper, therefore, is to serve as a vehicle of systematic review of DI-O₃ water applications and their benefits in wafer

surface preparation processes, with an intention of drawing more attention and discussion from the IC manufacturing industry on utilizing this technology in commercial application. The details of all the fundamental theories and operational procedures, however, are not included in the scope of the discussion.

SURFACE PASSIVATION

In theory, it was preferred to rinse wafers after the HF-last clean with DI water not containing dissolved oxygen to maintain an ultraclean, oxide-free silicon surface [3]. However, since the ultraclean surface in practice is not easy to maintain after the cleaning steps, more investigators have suggested to use ozonated

water for wafer rinsing to prevent subsequent contaminant deposition prior to the process of gate oxide growth [4-6]. The hydrogenated silicon surface after HF processes is susceptible to hydrocarbon adsorption and particle contamination. Passivating the silicon surface with a protective thin oxide film can significantly reduce the chance of contamination through wafer transportation in air ambient and minimize wafer surface micro-roughness during the heat-up stage in the gate-oxidation furnace, accordingly resulting in better gate oxide integrity (GOI) [7,8].

For example, Tardif and co-workers [9] have demonstrated that a 6- to 10-minute passivation step in 3 ppm DI-O₃ water can improve the breakdown charges (QBD) reproducibly of 7 nm gate oxide than does the HF-last only process (Fig. 2). In addition, they also found that proper DI-O₃ passivation can reduce the density of high roughness peaks at wafer surface and increased the QBD performance [10].

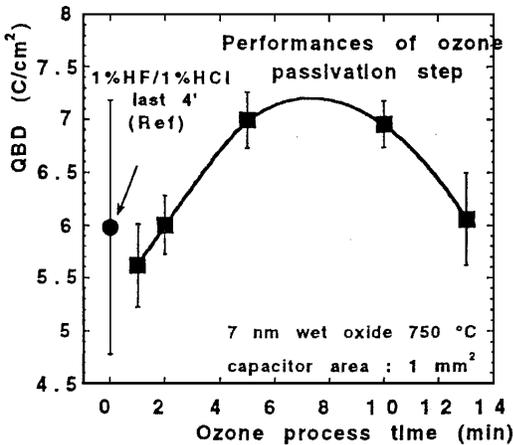


Figure 2. Comparison of QBD performance for samples receiving HF-last and DI-O₃ water treatments. (Ref. 9)

On the other hand, comparing the effect of passivation oxides formed by different chemicals (SPM, APM, HPM, hot H₂O₂, O₃-DIW, etc.) has shown that DI-O₃ water treatments produce the best GOI in terms of dielectric breakdown characteristics or cumulative failure density [7,8], as illustrated in Fig. 3. These results were attributed to the reproducible oxidation process by DI-O₃ water at room temperature, compared to the relatively poor control of oxide growth in other chemicals where the chemical concentration was changing by the evaporation and decomposition at elevated temperatures. Other than the influence of process control, the chemical oxide formed in ozonated water actually has better qualities, by showing less voids and the smoother interface, than those formed in APM, H₂O₂ solutions and even by HF-last steps [11], which are surely important for obtaining good GOI.

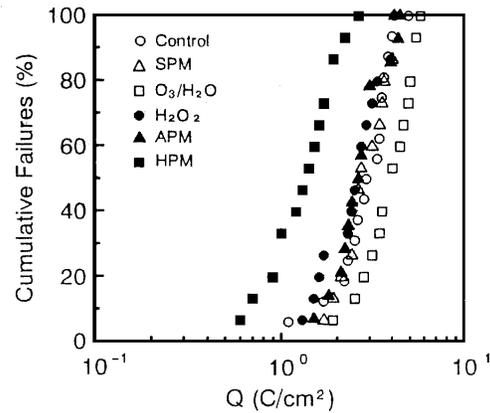


Figure 3. Cumulative failure characteristics of MOS diodes negatively biased with constant current density, which contained 6 nm gate oxide incorporating chemical oxides formed by various chemicals. (Ref. 7)

In addition, ozonated DI water has also been used after the HF last step to prevent the formation of watermark defects on silicon wafers [8,12]. Due to the highly hydrophobic and reactive characteristics of silicon surfaces after HF-last treatment, improperly drying the wafer can cause local oxidation of silicon surfaces by the oxygen dissolved in residual water drops after the drying process, especially on pattern features. The presence of this hydrated oxide residue (water marks) on the dried hydrophobic surface would degrade GOI because of the formation of locally thicker oxides after the gate oxidation process. It also can cause thickness and concentration variations after the implantation, CVD, or plasma etch process and results in the yield loss. By applying DI-O₃ water in final cleaning to passivate wafer surfaces, watermark defects can be significantly reduced, and the breakdown field

would shift to higher values than that after the HF-last-only step [8,12].

WAFER CLEANING

Silicon wafer cleaning in semiconductor device manufacturing includes a broad range of applications, such as IC pre-diffusion clean, IC pre-gate clean, IC oxide CMP clean, silicon post-polish clean, etc. These applications in general covers following fundamental processes; 1). removal of organic impurities, 2). removal of metallic contaminants, 3). removal of particles, and 4). removal of native oxide. Among them, the native oxide removal cannot be accomplished by DI-O₃ water alone, but ozone technology can regrow a clean oxide on bare silicon to suit some process requirements, as described in the previous section. For the other processes, DI-O₃ water can either work alone or be integrated with other chemicals to achieve the cleaning purposes. By and large, the ozone-involving applications have proven to be equally effective to the conventional RCA cleaning techniques.

Removal of Organic Impurities

It is well recognized that the removal of organic impurities from wafer surfaces is critical for the efficiency of subsequent chemical processes and the product performance/yield [13-15]. However, since polymeric materials are extensively used in the cleanroom, the outgassing of volatile organics from these materials may inevitably become a major source of the contamination. With its strong oxidizing power, ozonated DI water has been reported to be very efficient, as compared with other cleaning chemicals, in removing the airborne hydrocarbon contaminants from wafer surfaces [13,16,17]. As indicated by Fig. 4, two organic additives (BHT and DBP), which are commonly outgassed from wafer storage boxes, adsorbed on the wafer surface were fully removed by DI-O₃ water or dilute HF, while the APM, SPM and HNO₃ clean did not show equivalent efficiency [16]. Similarly, volatile hydrocarbon contaminants condensed on silicon wafers in the cleanroom environment were efficiently removed by ozonated DI water, especially at relatively high O₃ concentrations such as 20 ppm [17].

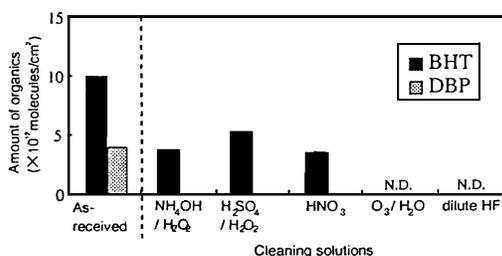


Figure 4. Amounts of organic contaminants adsorbing on wafer surfaces before and after wet cleaning by various chemicals. (Ref. 16)

In addition to the removal of trace amounts of organic contaminants, ozonated DI water has also shown its ability to remove significant amounts of organic compounds used in semiconductor technology, such as surfactants added to the developer in the lithography process [18] and the HexaMethylDiSilaxane (HMDS) photoresist primer [19]. Moreover, the technology of using DI-O₃ water for photoresist removal has also been developed recently, and the detail will be reviewed and discussed separately in a succeeding section.

Removal of Metallic Contaminants

The use of DI-O₃ water has been found effective in removing detrimental metals such as Cu and Ag on wafer surfaces [9,20,21]. These metals are verified as noble metals because they have higher electronegativity than Si and readily reduce at wafer surfaces by oxidizing silicon. It was found that concentrations of these metals on pre-contaminated wafers dropped from 10¹³ atoms/cm² to the order of 10¹⁰ atoms/cm² in 3 ppm ozonated water in 5 minutes [9,20], as shown by Fig. 5. It was also noted that the mixture of 0.01% HCl with the ozonated DI water accelerated the Cu removal, but induced high Ag concentrations by the re-precipitation of AgCl particles to the wafer surface [9,20].

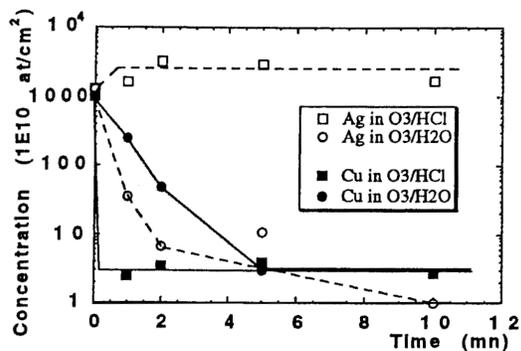


Figure 5. Cu and Ag removal by dilute ozone chemistries as measured by TXRF. (Ref. 9)

In addition, it has been observed that longer dip time and higher ozone concentration both produce

more thorough Cu removal than conventional SC2 [21] (Figure 6).

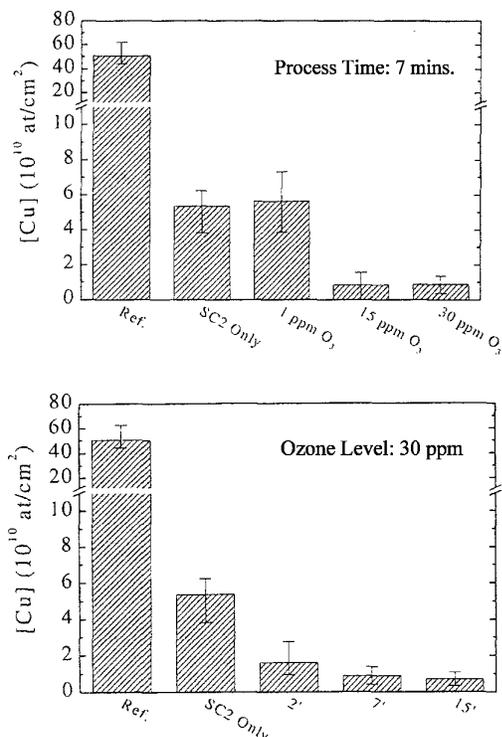


Figure 6. Cu removal by 1:1:5 SC2 at 65°C versus DI-O₃ water with various dip time and ozone concentration; (Top) effect of ozone level and (Bottom) effect of dip time. (Ref. 21)

However, ozonated DI water alone is not effective in removing transition metals (e.g. Fe, Ni, etc.), Al and alkaline-earth metals (e.g. Ca, Mg, etc.). These metallic contaminants can deposit on silicon surfaces in the forms of metal hydroxides and/or metal oxides, or the metal oxides may incorporate into the native oxide of hydrophilic wafers. In these circumstances, oxidizing acid solutions and oxide stripping steps are therefore required to eliminate the metallic contaminants from silicon surfaces, which have led to the onset of using HF/HCl chemistries for removing transition and alkaline metals such as the diluted dynamic clean (DDC) technique [9,10,20,22]. On the other hand, some researchers have combined DI-O₃ with HF to demonstrate the effectiveness in removing both noble (Cu) and transition (Fe, Ni) metals by the simultaneous oxidizing and stripping effect [23]. This technique, although promising, needs careful control of the chemical concentrations since re-deposition of Cu would occur as HF concentration exceeds critical values [23,24].

Removal of Particles

Although viewed as an attractive candidate with the strong oxidizing power, by no means is O₃ able to

replace H₂O₂ in the APM solution due to the difficulty of establishing sufficient ozone concentration in alkaline solutions [25] and at elevated temperatures (say 50°C or higher) [9]. The reaction between ozone and hydroxyl ions not only consumes dissolved O₃ but also decreases the solution pH, totally eliminating the favorable power of APM chemistry in terms of oxide growth/etch mechanism and Zeta potential advantage. A different approach is the use of HF/O₃ mixture, in which the HF etches SiO₂ while ozone simultaneously grows fresh oxides from silicon surface; a way of mimicking the functions of ammonia and hydrogen peroxide in the SC1 clean [23]. Unlike APM solutions, however, the HF/O₃ solutions are relatively difficult to control to maintain reliable process robustness without causing unacceptable damages to the silicon wafer. In addition, this chemistry does not provide favorable pH ranges to keep most particles and Si surface in the same polarity for efficient particle removal. An alternative was proposed using separated HF and DIW/O₃ steps for particle removal [20,21,26,27]. The process is based on a concept of removing particles by etching the silicon oxide that is firstly formed in ozonated water. Moreover, diluted HCl can be added to the HF solution to drive the pH value below 2; a range believed to be favorable for obtaining proper Zeta potentials in particle removal. As shown in Fig. 7, 10-minute rinse in DI-O₃ water (3 ppm) followed by dipping in so-called “%” solution (e.g. 1:1:100 HF/HCl/DIW) produces particle removal efficiency better and faster than 1:100 HF alone [9,20]. On the other hand, by alternating the DIW/O₃ and diluted HF step repeatedly, the removal efficiency of stubborn particles such as alumina (Al₂O₃) can gradually increase to about 90% [27].

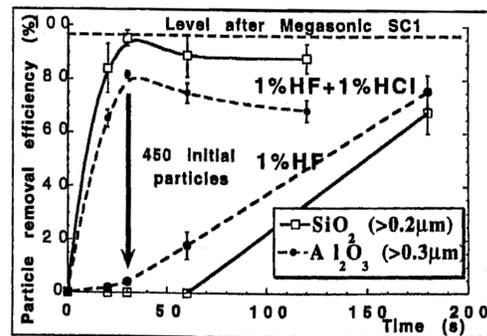


Figure 7. Particle removal efficiency of SiO₂ and Al₂O₃ by 10-minute DIW-O₃ (3 ppm) rinse followed by diluted HF/HCl or HF dip. (Refs. 9,20)

Diluted Dynamic Clean (DDC)

Under the incentive of process efficiency and chemical saving, HF/O₃-chemistry-based wet cleaning techniques have been recently proposed by

different researchers, such as IMEC clean by Heyns [28], diluted dynamic clean (DDC) by Tardif [20], and ultra clean technology (UCT) by Ohmi [29]. Herein, DDC technique is used as an example to summarize the concepts and to show the economic benefits of using HF/O₃ chemistry in the wet cleaning of silicon wafers. Table 1 indicates the general concept and process steps of DDC adapted to pre-gate cleaning.

Table 1: DDC concept adapted to pre-gate cleaning

Process (20°C)	Time (min.)	Bath	Goal
O ₃ 20 ppm	5	Dyn.	CH _x + noble metals
% solution: 1%HF + 1%HCl	0.5	Recir.	Sac. Ox. + metals
Rinse	1	Dyn.	Rinse
O ₃ 3 ppm	10	Recir.	Particle Removal
% solution: 1%HF + 1%HCl	1		
Rinse w/ 0.01%HCl	1	Dyn.	Rinse
O ₃ 3 ppm w/ 0.01%HCl	7		Final Passivation
Total:	26.5		

It is a dual tank system with “%” solution in the recirculation mode and DI-O₃ water in the dynamic mode (single-path). The first step of DI-O₃ water treatment is designated to remove hydrocarbons and noble metals. Then the sacrificial oxide and ionic contaminants are removed in the “%” solution, followed by rinsing off the traces of HF. Afterwards, 10-minute injection of ozone grows a chemical oxide under the particles, and the particles are removed by the same “%” solution through the under-etching mechanism. The wafers are then rinsed for 1 minute before the final ozone passivation step. The use of trace of HCl during the two final rinsing steps prevents metallic re-contamination from the DI water. The drying sequence is not included in the table because it is not particularly a cleaning step and is in general required for most of the wet processes.

Systematic studies have been conducted on both full sheet and patterned wafers with a commercial automated wet bench to compare the cleaning performance of DDC, dRCA (diluted SC1 & SC2), aRCA (advanced RCA; i.e. diluted SC1 + HF/O₃ chemistry), and conventional RCA (SC1 & SC2) in the aspects of particle removal efficiency, metal removal efficiency, surface characteristics, electrical QBD tests [30]. Experimental results indicated that

the advanced processes were at least as good as (more often better than) the RCA process. Actually, three-year data collection from the same wet bench for gate oxides between 4.5 and 7 nm on epi or bulk wafers, using dry or wet oxidation process, has shown a consistent correlation of getting good intrinsic electrical performances of the gate oxides with DDC versus a conventional RCA full clean (SPM/HF/SC1/SC2) [10]. Figure 8 shows an example of the monitoring results after using the full RCA clean and DDC in parallel on the same wet bench, statistically proving the interest of DDC.

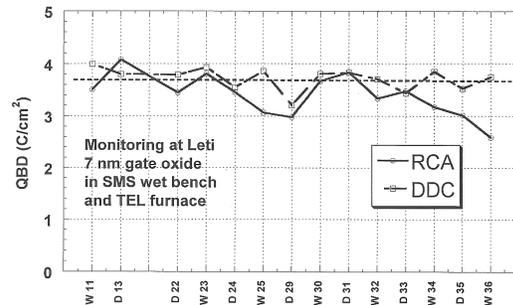


Figure 8. Monitoring results obtained between RCA and DDC cleanings performed in parallel on the same wet bench, followed by alternative dry and wet gate oxidation processes. (Ref. 10)

Furthermore, the DDC process provides additional advantages compared to RCA clean, such as higher throughput (~30 minutes versus > 1 hour of processing) and smaller footprint (dual tanks versus 8 tanks or more). Also, the long-term monitoring has demonstrated the superior cost-effectiveness of DDC against the conventional SPM/HF/RCA; i.e. reducing chemicals' consumption by 8 to 40 times (according to the throughput: respectively 7200 and 1200 wafers/day) and saving DI water by 3 times (bath lifetime: 24 hours) [10,20].

PHOTORESIST STRIPPING

In recent years, one of the most exciting technological developments in semiconductor wet cleaning industry may be the trial of utilizing ozone chemistry for photoresist removal to eliminate the sulfuric acid based stripping procedure. Used in IC manufacturing sequence for more than 20 years, sulfuric acid has earned its longevity for many reasons. As a cleaning agent, it effectively removes both organic and inorganic residues. As a medium for stripping developed photoresist from non-metallized surfaces following the etching and implantation steps, sulfuric acid has proven to be fast and thorough. While contributing significantly to the IC production sequence, sulfuric based steps have revealed several drawbacks, such as the great consumption of expensive chemicals, unstable bath

conditions, requirement of vast amounts of DI water for rinsing, highly dangerous processes, etc. The use of ozone, on the contrary, is not subject to these concerns.

The initial ozone application in photoresist stripping results from the intention of replacing hydrogen peroxide used in the SPM solution for a cost-saving purpose [31,32]. The SPM process requires periodic replenishing of H_2O_2 (an expensive chemical) and frequent bath change-out to maintain the stripping effectiveness of the Caro's acid (i.e. H_2SO_5), while ozone can be continuously generated from oxygen gas and purged into the sulfuric acid to produce a relatively strong and stable oxidizing agent (i.e. dipersulfuric acid, $H_2S_2O_8$) for resist stripping [31,32]. A comparison of the two chemistries has revealed that SOM (i.e. $H_2SO_4 + O_3$) can efficiently oxidize batches of ashed wafers at a lower operating temperature (e.g. $90^\circ C$) for up to a week (versus a typical lifetime of 8~12 hours for SPM baths) without sacrificing the resist stripping performance [31,32].

Though proven to be more cost-effective than SPM, the SOM process still needs to use sulfuric acid at high temperatures followed by DI water rinse, which is inevitably associated with many hidden costs, safety issues and environmental concerns. In this regard, a simple DIW/ O_3 chemistry has been developed for resist removal to eliminate the problems [33-35]. In order to be well integrated with the conventional wet bench system, the novel technology was developed on the basis of immersion techniques. Systematic experiments have been conducted to evaluate the process and the results are promising for the commercial application [33-35].

With its highly oxidizing power, ozone dissolved in DI water reacts with the hydrocarbon in polymers, forming CO_2 and H_2O , and removes photoresist, accordingly. Unlike the stripping action from sulfuric mixtures, in which the resist is softened and undercut by the sulfuric acid, the DIW/ O_3 process directly oxidizes the resist from the wafer surface; the resist is continually thinned in a manner similar to the etching effect of hydrofluoric acid solutions on silicon dioxide. The process bath remains "clear" during the entire process time, in contrast to the SPM and SOM solutions that would turn brown from the presence of un-oxidized organic materials.

It has been well known that the solubility of ozone in DI water decreases with the increase of water temperature. Also, it is clear that the presence of sufficient amounts of reactants is required for the reaction kinetics enhancement. The premises had

led to the onset of Chilled-DIO 3^{TM} technology for resist stripping [33-36]. As shown in Figure 9, the maximum ozone concentration can be built up to 80 ppm in a $5^\circ C$ DI- O_3 water bath and achieves a strip rate of 65 nm/min, while the strip rate would be reduced if the dissolved O_3 concentration decreases [35].

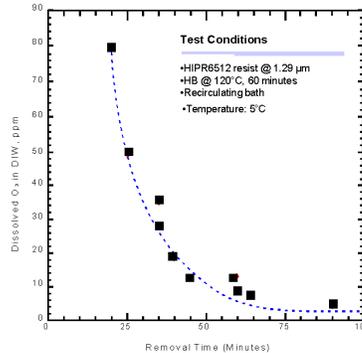


Figure 9. Dissolved ozone concentration versus the total strip time of a 1.29- μm photoresist. (Ref. 35)

However, recent research has shown that increasing the bath temperature, although reducing the ozone concentration in water, does not necessarily slow down the resist stripping [37]. Figure 10 shows the variations of resist strip rate and dissolved ozone concentration as a function of process temperature. It can be seen that the strip rate of the Shipley SPR2 resist can be maintained at 65 nm/min as the DI- O_3 water is heated to $35^\circ C$ (i.e. $[O_3] \approx 23$ ppm). This is most likely due to the increase of reaction/diffusion rate at elevated temperatures to compensate the loss of ozone concentration in the system.

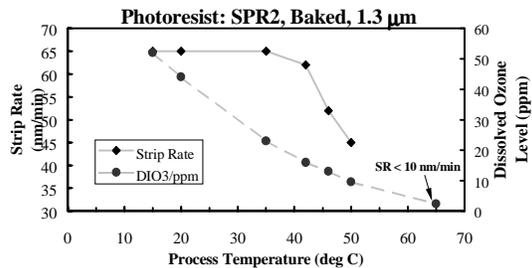


Figure 10. The variations of resist strip rate and ozone concentration in the DIW/ O_3 process as a function of the process temperature. (Ref. 37)

The DIW/ O_3 process has also proven to be applicable for the removal of a wide variety of photoresist except the negative resist and highly implanted positive resist ($\geq 1.0E+15$ atoms/cm 2). As shown in Fig. 11, three types of photoresist with different thickness (i.e. AZ1518 (A), HIPR6512 (B) and Shipley SPR2 (C)) stripped by ozonated DIW at $10^\circ C$ ($[O_3] \approx 65$ ppm) exhibit strip rates from 50 to 65 nm/min, also indicating that etch rates attained

by the process is not significantly influenced by the resist type [33-35].

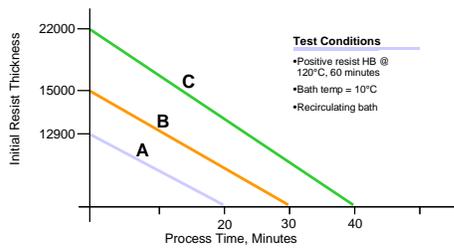


Figure 11. Etch rates in DIW/O₃ processing for different types of photoresist (A: AZ1518, B: HIPR6512, C: Shibley SPR2). (Ref. 35)

Experimental results have also indicated the superior performance of ozone process compared to sulfuric acid mixtures in terms of process contamination. Particle addition to bare silicon wafers through DIW/O₃ has been investigated [33-35], and the result shows an average of 12 particles per wafer (PPW) adding at 0.2 μm and about 23 PPW adding at 0.16 μm (Fig. 12). Table 2 gives the metal level and particle count found on wafer surfaces following the SPM, SOM or DIW/O₃ processing.

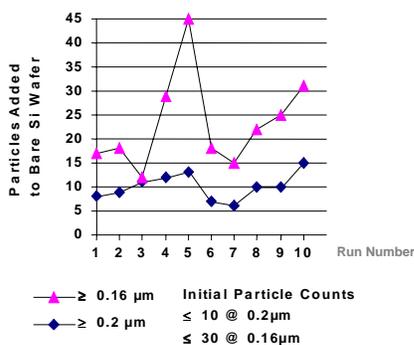


Figure 12. Particle counts on bare Si surfaces after the DIW/O₃ resist stripping process. (Ref. 35)

Table 2: Process performance from SPM, SOM, and DIW/O₃ processes. (Ref 35)

Element Process	METALS COMPARISON ⁽¹⁾					PARTICLES COMPARISON ⁽²⁾	
	S	K	Ca	Fe	Cu	≥ 0.16 μm	≥ 0.2 μm
H ₂ SO ₄ :H ₂ O ₂	148.5	ND	0.19	0.11	0.22	453	189
DIO3™	5.5	0.06	0.17	0.25	0.06	53	21
H ₂ SO ₄ :O ₃	467.5	0.06	0.14	0.17	0.03	439	327

⁽¹⁾ Units (10¹⁰ atoms/cm²). Measured via VPD-DSE-TXRF [6].
⁽²⁾ Measurements taken 4 hours after Process.

Note that the particle measurements are taken after 4-hour cleanroom storage after the stripping processes. The high particle counts of the sulfuric treated wafers are essentially associated with the time-dependent hazing induced by sulfate residues. The results show much lower particle contamination for the DIW/O₃ processing than those resulting from SPM, SOM methods, suggesting that the DIW/O₃ technique is an inherently clean, rinse-free process compared to its sulfuric acid counterparts. Although viewed as a “clean” process, DIW/O₃ is not a cleaning step. Therefore, an SC1 step following the ozone resist stripping is recommended to eliminate possible resist residues located at the critical area and to meet the tight particle specification in today’s IC device manufacturing.

Since the DIW/O₃ process does not require post-process rinsing, there is a saving of 99.5% of the water consumption compared to the sulfuric chemistries [35]. Even taking into account the subsequent SC1 cleaning step, the ozone technique can still save DI water by about 70%, not to mention other associated advantages such as reduced chemical consumption, increased hardware life, reduced downtime for bath change-out, reduced bench footprint and equipment costs, and improved safety and environmental conditions. Cost of ownership analysis between the sulfuric based and ozone-DI water based methods for a typical process that produces 4 lots (50 x 200 mm wafers) per hour has shown that a minimum cost reduction of about 60% can be obtained by using the DIW/O₃ technique [34].

As the research in DIW/O₃ resist stripping continues to proceed, different approaches from immersion techniques have been taken and also showed interesting results [38-40]. These techniques, based on either boundary layer control or mass transfer control theory, use ozone-moisture environments or DI-O₃ water spraying in conjunction with wafer spinning to achieve the desired conditions for resist stripping. Although enhancing the intrinsic stripping-kinetics, the non-immersion techniques in

general have not shown significant difference from the immersion method in terms of overall process performance. Vroom and De Gendt have investigated the resist strip with commercial tools from wet bench vendors using the three advanced aqueous ozone techniques versus the conventional SPM method [41]. All the results were compared in the aspect of process time, oxide thickness, total organic contamination (TOC), metal contamination, yield, defect density, and GOI. The conclusion was that there is no significant difference in performance among the ozone processes and the standard SPM process [41], once again proving the commercial viability of DIW/O₃ in resist stripping and cleaning.

CONCLUSION

The application of ozone in semiconductor wet cleaning has been reviewed, based on the work performed by researchers in past years. The results indicated that ozone is a powerful oxidant and can provide economic benefits in wafer surface preparation. The application of ozone technology on wafer cleaning and photoresist stripping has shown superior, or at least equivalent, performance compared to the conventional SPM/RCA process. Due to its simplicity, the wet ozone process can be implemented onto existing production tools without major modifications. The author would like to suggest that more efforts on “ β -testing” of the ozone processes should be taken under the collaboration between the equipment and the IC manufacturing industry to pilot the novel technology to fully accepted commercial applications.

REFERENCES

[1] W. Kern, Handbook of Semiconductor Wafer Cleaning Technology, (ed., W. Kern), Noyes Publications, Westwood, NJ, 1993, p. 3.

[2] T. Ohmi, in Cleaning Technology in Semiconductor Device Manufacturing IV, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1996, pp. 1-12.

[3] K. Yabe, Y. Motomura, H. Ishikawa, T. Mizuniwa and T. Ohmi, *Microcontamination*, 7 (2), 1989, pp. 37-46.

[4] W.C. Krussell and D.I. Golland, in Cleaning Technology in Semiconductor Device Manufacturing I, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1990, pp. 23-32.

[5] S. Nelson, in Semiconductor Pure Water and Chemical Conference 1996 Proceedings, (ed., M.K. Balazs), Balazs Analytical Laboratory, 1996, pp. 230-242.

[6] L. Li, W. Lee, T. Gilton and F. González, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 272-279.

[7] K. Nakamura, T. Futatsuki, K. Makihara and T. Ohmi, in Cleaning Technology in Semiconductor Device Manufacturing III, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1994, pp. 70-77.

[8] J.-G. Park, *Jpn. J. Appl. Phys.* 36 (9A), 1997, pp. 5416-5420.

[9] F. Tardif, T. Lardin, P. Boelen, R. Novak and I. Kashkoush, in Ultra Clean Processing of Silicon Surfaces, (eds., M. Heyns, M. Meuris and P. Mertens), Acco, Leuven (België), 1996, pp. 175-178.

[10] F. Tardif, T. Lardin, Y. Abolafia, A. Danel, P. Boelen, C. Cowache, I. Kashkoush and R. Novak, in Ultra Clean Processing of Silicon Surfaces, (eds., M. Heyns, M. Meuris and P. Mertens), Scitec Publications Ltd, Zuerich-Uetikon (Switzerland), 1998, pp. 19-22.

[11] T. Ohwaki, M. Takeda and Y. Takai, *Jpn. J. Appl. Phys.* 36 (9A), 1997, pp. 5507-5513.

[12] J.-G. Park and M.F. Pas, in Cleaning Technology in Semiconductor Device Manufacturing IV, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1996, pp. 82-89.

[13] T. Ohmi, in Cleaning Technology in Semiconductor Device Manufacturing III, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1994, pp. 3-14.

[14] F. Tardif, G. Quagliotti, T. Baffert and L. Secourgeon, in Ultra Clean Processing of Silicon Surfaces, (eds., M. Heyns, M. Meuris and P. Mertens), Acco, Leuven (België), 1996, pp. 309-312.

[15] T. Hattori, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The

- Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 3-14.
- [16] K. Saga and T. Hattori, in Ultra Clean Processing of Silicon Surfaces, (eds., M. Heyns, M. Meuris and P. Mertens), Acco, Leuven (België), 1996, pp. 299-303.
- [17] E. Ollier, S. Marthon, G. Quagliotti and F. Tardif, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 447-454.
- [18] T. Ohmi, T. Isagawa, M. Kogure and T. Imaoka, *J. Electrochem. Soc.*, 140 (3), 1993, pp. 804-810.
- [19] C. Kenens, S. De Gendt, D.M. Knotter, L.M. Loewenstein, M. Meuris, W. Vandervorst and M. Heyns, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 247-255.
- [20] F. Tardif, T. Lardin, B. Sandrier, P. Bolen, R. Matthews, I. Kashkoush and R. Novak, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 15-22.
- [21] F. Pipia, E. Bellandi, B. Crivelli and M. Alessandri, in Ultra Clean Processing of Silicon Surfaces, (eds., M. Heyns, M. Meuris and P. Mertens), Scitec Publications Ltd, Zuerich-Uetikon (Switzerland), 1998, pp. 109-112.
- [22] F. Tardif, T. Lardin, C. Paillet, J-P. Joly, A. Fleury, P. Patruno, D. Levy and K. Barla, in Cleaning Technology in Semiconductor Device Manufacturing IV, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1996, pp. 49-59.
- [23] Y. Fukazawa, K. Miyazaki and Y. Ogawa, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 264-271.
- [24] H. Morita, J.-D. Joo, R. Messoussi, K. Kawada, J.-S. Kim, T. Ohmi, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 143-150.
- [25] J.-G. Park and J.-H. Han, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 231-238.
- [26] M. Alessandri, E. Bellandi, F. Pipia, F. Cazzaniga, K. Wolke and M. Schenkl, in Ultra Clean Processing of Silicon Surfaces, (eds., M. Heyns, M. Meuris and P. Mertens), Scitec Publications Ltd, Zuerich-Uetikon (Switzerland), 1998, pp. 27-30.
- [27] T. Osaka, A. Okamoto, H. Kuniyasu and T. Hattori, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 256-263.
- [28] M. Meuris, S. Verhaverbeke, P.W. Mertens, H.F. Schmidt, A.L.P. Rotondaro and M.M. Heyns, in Cleaning Technology in Semiconductor Device Manufacturing III, (eds., J. Ruzyllo and R.E. Novak), The Electrochemical Society, Inc., Pennington, NJ, 1994, pp. 15-25.
- [29] T. Ohmi, *J. Electrochem. Soc.*, 143 (9), 1996, pp. 2957-2964.
- [30] C. Cowache, P. Boelen, I. Kashkoush, P. Besson and F. Tardif, in The Sixth International Symposium on Cleaning Technology in Semiconductor Device Manufacturing, Honolulu, HI, Oct. 18-20, 1999.
- [31] J. Wei, G. Smolinsky, S. Verhaverbeke and J. Parker, in Semiconductor Pure Water and Chemical Conference 1996 Proceedings, (ed., M.K. Balazs), Balazs Analytical Laboratory, 1997, pp. 81-97.
- [32] J. Wei and S. Verhaverbeke, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 496-504.
- [33] I. Kashkoush, R. Matthews, R. Novak, E. Brause, F. Carrillo and B. Rajaram, in Materials Research Society Symposium Proceedings, Vol. 477, (eds., G.S. Higashi, M. Hirose, S. Raghavan and S. Verhaverbeke), Materials

- Research Society, Pittsburgh, PA, 1997, pp. 173-178.
- [34] I. Kashkoush, R. Novak, R. Matthews and M. Lamarra, *Future Fab International*, Vol. 1, Issue 3, Technology Publishing Ltd., London, UK, 1997, pp. 249-254.
- [35] I. Kashkoush, R. Matthews and R. Novak, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 471-479.
- [36] M. Dax, *Semiconductor International*, October 1996, p. 74.
- [37] J. Cheng, D. Nemeth, G. Chen and I. Kashkoush, "A Study of Temperature Effect in Photoresist Stripping with DIO₃ Process", Technical Report, AKrion, Allentown, PA, April 12, 1999.
- [38] S. De Gendt, J. Wauters and M. Heyns, "A Novel Resist and Post-Etch Residue Removal Process Using Ozonated Chemistry", *Solid State Technology*, December, 1998, pp. 57-60.
- [39] K. Christenson, S. Nelson, M. Olim and G. Nelson, in Cleaning Technology in Semiconductor Device Manufacturing V, (eds., R.E. Novak and J. Ruzyllo), The Electrochemical Society, Inc., Pennington, NJ, 1998, pp. 480-487.
- [40] S. Nelson, "Ozonated Water for Photoresist Removal", *Solid State Technology*, July, 1999, pp. 107-112.
- [41] R. Vroom and S. De Gendt, in The Eighth Intl. Symposium on Semiconductor Manufacturing, Santa Clara, CA, Oct. 11-13, 1999.

AUTHOR BIOGRAPHY

Gim S. Chen holds a Ph.D. in Materials Science and Engineering and has been working at AKrion (formerly SubMicron Systems) for 2 years as Process Engineer in wet cleaning process development.